PATENT ABSTRACTS OF JAPAN

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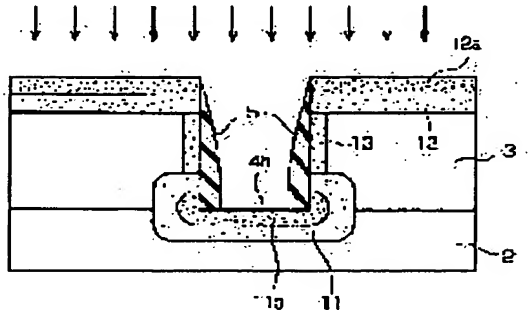
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE EQUIPPED WITH VERTICAL TRANSISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method of manufacturing a semiconductor device equipped with a vertical transistor, wherein an LDD can be surely provided to a vertical transistor, and the vertical transistor can be controlled in threshold voltage.
SOLUTION: A vertical transistor equipped with a channel region which extends along an inner wall of a groove vertical to a substrate 2 is manufactured as follows: Ions are implanted into the substrate 2 at a right angle to form offset regions 11 and 12 which serve as LDD, a side wall 5 is formed on each inner wall of the groove, and then ions are implanted into the side walls for the formation of source-drain regions. By this setup, the source.drain regions can be easily formed as self-aligned with LDD(Lightly Doped Drain). A vertical transistor of this constitution can be controlled in threshold voltage by a process where ions are obliquely implanted into the substrate 2.



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